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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,066	09/28/2000	Charles P. Roth	10559-293001/P9300-ADI	2845

20985 7590 11/03/2003

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,066	ROTH ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The section entitled "Description of Drawings" in the specification is objected to for not containing a description of Figures 5 and 6. Appropriate correction is required.

Claim Objections

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12 and 13 are objected to under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. In claim 12, line 6, the limitation "the references" lacks antecedent basis. Please change the limitation "the references" to -- references --.

6. In claim 13, line 2, the limitation "the pair" lacks antecedent basis. Please change the limitation "the pair" to -- a pair --.

7. In claim 13, line 8, the limitation "the remaining" lacks antecedent basis. Please change the limitation "the remaining" to -- remaining --.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, 4, 6, 9, and 10 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as element "AA" in the IDS submitted by Applicant on May 21, 2002.

10. Referring to claim 1, Kobayashi et al. have taught a method comprising:

a. receiving a machine instruction directing a processor to search a plurality of data elements (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65); and executing the machine instruction by:

b. retrieving M data elements in a single fetch cycle (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65, When M=1.);

c. concurrently comparing the M data elements to a corresponding current extreme value (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65, elements 3321 and 3322, Where M=1.); and updating a set of references based on the comparisons (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65, Where M=1.).

11. Referring to claim 2, Kobayashi have et. have taught the method of claim 1, as described above, and wherein retrieving the M data elements comprises retrieving the M data elements as a single data quantity containing the M data elements (Kobayashi at al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65).

12. Referring to claim 4, Kobayashi et al. have taught the method of claim 1, wherein M = 1 (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65).

13. Referring to claim 6, Kobayashi et al. have taught the method of claim 1, wherein executing the machine instruction further includes:

a. storing the current extreme values in M accumulators (Kobayashi et al., Column 5, lines 1-65); and

b. copying the M data elements to the accumulators based on the comparisons (Kobayashi et al., Column 5, lines 1-65).

14. Referring to claim 9, Kobayashi et al. have taught the method of claim 1, as described above, and wherein concurrently comparing each of the data elements to a current extreme value includes determining whether each of the data elements is less than the corresponding current extreme value (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65).

15. Referring to claim 10, Kobayashi et al. have taught the method of claim 1, as described above, and wherein concurrently comparing each of the data elements to a current extreme value includes determining whether each of the data elements is greater than the corresponding current extreme value (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65).

16. Claims 13, 14, and 15 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002.

17. Referring to claim 13, Oberman et al. have taught a method comprising:

a. retrieving the pair of data elements from an array of elements in a single fetch operation, wherein the pair of data elements includes an even data element and an odd

data element (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, elements 3182A, 3182B, 204A, 204C, Element 204A is the even data element and 204C is the odd data element.);

b. substantially comparing the even element of the pair and the odd element of the pair (Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The element 204A is the even data element that is compared with 204C, the odd data element.); and

c. substantially fetching and comparing the remaining pairs of data elements of the array until all of the data elements of the array have been processed (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204, B, 204D, The elements 204B and 204D are the remaining pair of data elements that are fetched and compared.).

18. Referring to claim 14, Oberman et al have taught the method of claim 13, as described above, and wherein substantially comparing the pair of data elements includes setting an even minimum value as function of the even element of the element pair (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204, B, 204C, 204D, The even minimum value, element 3008A, is set by comparing 204A with 204C.) and setting an odd minimum value as function of the odd element of the element pair (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204, B, 204C, 204D, The odd minimum value, element 3008B, is set by comparing 204B with 204D.).

19. Referring to claim 15, Oberman et al. have taught the method of claim 13, as described above, and wherein substantially comparing the pair of data elements includes maintaining a first accumulator to store a minimum value for the even elements (Figure 50, element 3008A) and a second accumulator to store a minimum value for the odd elements (Figure 50, element 3008B).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as element "AA" in the IDS submitted by Applicant on May 21, 2002, in view of Stroustrup.

22. Referring to claim 3, Kobayashi et al. have taught the method of claim 2, as described above. Kobayashi et al. have not specifically taught wherein the set of references comprise pointer registers to store addresses for data quantities. However Stroustrup has taught that a set of references comprise pointer registers to store addresses for data quantities (Stroustrup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays") in order to efficiently and elegantly handle traversing an array. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of references, as taught by Kobayashi et al., comprise pointer registers to store addresses for data, as taught by Stroustrup (Stroustrup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays"), for the desirable purpose of efficiently and elegantly searching arrays.

23. Claims 5, 7, 8, 11, 12, 19, 20, 21, 22, 23, 26, 27, 28, 29, 30, 31, 33, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as element "AA" in the IDS submitted by Applicant on May 21, 2002, in view of Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002.

24. Referring to claim 5, Kobayashi et al have taught the method of claim 1, as described above. Kobayashi et al. have not specifically taught wherein M = 2. However, Oberman et al. have taught FPMAX and FPMIN instructions that concurrently compare multiple data elements such that M=2 in order to increase parallelism (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al. concurrently compare multiple data elements such that M=2, as taught by Oberman et al., for the desirable purpose of increasing parallelism which speeds up overall execution.

25. Referring to claim 7, Kobayashi in combination with Oberman et al. have taught the method of claim 5, as described above, and wherein concurrently comparing the data elements comprises processing a first data element with a first execution unit of a pipelined processor (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 136C/D) and processing a second data element with a second execution unit of the pipelined processor (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 136C/D).

26. Referring to claim 8, Kobayashi et al. have taught the method of claim 5, as described above, and wherein concurrently comparing the data elements comprises concurrently processing a first data element and a second data element within a single execution unit of a pipelined processor (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 136C, For the PFMIN and PFMAX instructions, the pipelines each receive two operands to be compared.).

27. Referring to claim 11, Kobayashi has taught a method for searching an array of N data elements for a value (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65) comprising:

a. issuing machine instructions to a processor (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65); and

b. analyzing results of the machine instructions to identify a value for the array (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65, Identify a minimum or maximum value.).

28. Kobayashi et al. have not specifically taught issuing N/M machine instructions to a processor, wherein the processor is adapted to process M data elements in parallel; and analyzing results of the machine instructions to identify a value for the array.

29. Oberman has taught issuing machine instructions to a processor, wherein the processor is adapted to process M data elements in parallel (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18); and analyzing results of the machine instructions to identify a value for the array (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, A minimum or

maximum value is determined.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al. include wherein the processor is adapted to process M data elements in parallel; and analyzing results of the machine instructions to identify a value for the array, as taught by Oberman, in order to increase parallelism per instruction which speeds up execution time.

30. While Kobayashi et al. may not have specifically taught issuing N/M machine instructions to a processor, Oberman has taught that the number of instructions are reduced for performing a certain operation when two data elements are compared in parallel. With Oberman we have two separate things that used to be implemented with two instructions, that are now being implemented with one instruction (FPMIN and FPMAX). Implementing half as many instructions of Kobayashi et al. is an obvious improvement in light of Oberman in order to increase instruction parallelism. For example, in the case of Oberman, M=2. If we have an array of Kobayashi of size 10, such that N=10, then 10/2 = 5 instructions would be required to search the array for an extreme value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al., issue N/M machine instructions to a processor, such that 2 times the amount of data is operated on in a single instruction, as taught by Oberman et al., so that ½ as many instructions of Kobayashi et al. need to be issued to search an array for an extreme value for the desirable purpose of increasing instruction level parallelism and execution time.

31. Referring to claim 12, Kobayashi et al. in combination with Oberman et al. have taught the method of claim 11, further comprising:

a. executing each machine instruction by:

b. retrieving M data elements in a single fetch cycle (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18), concurrently comparing each of the M data elements to a corresponding current extreme value (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Kobayashi et al., column 5, lines 44-65), and updating the references based on the comparisons (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, elements 3321 and 3322, Kobayashi et al., column 5, lines 44-65).

32. Claim 19 does not claim anything over claim 11 and is therefore rejected for the same reasons as claim 11.

33. Claim 20 does not claim anything over claim 12 and is therefore rejected for the same reasons as claim 12.

34. Referring to claim 21, Oberman has taught the apparatus of claim 19, as described above, and wherein the pipeline includes M registers adapted to store references to the extreme values (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 3008A and 3008B, elements 3321 and 3322).

35. Claim 22 does not claim anything over claim 3 and is therefore rejected for the same reasons as claim 3.

36. Referring to claim 23, Oberman has taught the apparatus of claim 21, as described above, and wherein the registers are general-purpose data registers (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 3008A and 3008B).

37. Claim 26 does not claim anything over claims 11 and 12 and is therefore rejected for the same reasons as claims 11 and 12.

38. Claim 27 does not claim anything over claim 12 and is therefore rejected for the same reasons as claim 12.

39. Claim 28 does not claim anything over claim 8 and is therefore rejected for the same reasons as claim 8.

40. Referring to claim 29, Kobayashi et al. in combination with Oberman et al. have taught the limitations of claim 29, as described in the rejection to claims 11 and 12, and a processor coupled to a memory device (Oberman, Figure 51, element 3404).

41. Claim 30 does not claim anything over claims 11 and 12 and is therefore rejected for the same reasons as claims 11 and 12.

42. Referring to claim 31, Kobayashi et al in combination with Oberman et al. have taught the system of claim 29, as described above, and wherein the pipeline includes M registers configured to store references to the extreme values (Kobayashi, column 5, lines 44-65, temporary register, Oberman, Figure 50, elements 3321 and 3322).

43. Referring to claim 33, Kobayashi et al in combination with Oberman et al. have taught the system of claim 31, as described above, and wherein the registers are general-purpose data registers (Kobayashi, column 5, lines 44-65, temporary register, Oberman, Figure 50, elements 3321 and 3322).

44. Referring to claim 34, Kobayashi et al. in combination with Oberman et al. have taught the system of claim 29, as described above, and wherein the memory device comprises static random access memory (Oberman et al., Page 57, lines 3-5).

45. Referring to claim 35, Kobayashi et al. in combination with Oberman et al. have taught the system of claim 29. While Kobayashi et al. in combination with Oberman et al. may not have taught wherein the memory device comprises FLASH memory, it is well known that flash memory is connected to processors for the purpose of providing nonvolatile memory to maintain data between sessions. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al. and Oberman et al. include a flash memory connected to the processor for the desirable purpose of providing nonvolatile memory to maintain data between sessions.

46. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as element "AA" in the IDS submitted by Applicant on May 21, 2002, in view of Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002, and in view of Stroustrup.

47. Claim 32 does not claim anything over claim 3 and is therefore rejected for the same reasons as claim 3.

48. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002, in view of Stroustrup.

49. Referring to claim 16, Oberman et al. have taught the method of claim 13, as described above. Oberman et al. has not specifically taught further including maintaining a first pointer register to store an address for the minimum value of the even data elements and maintaining a second pointer register to store an address for the minimum value of the odd data elements. However, Stroustroup has taught referencing data values using a pointer register while accessing

an array (Stroustroup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays") in order to efficiently and elegantly handle reference a value in an array of values. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the odd and even minimum values of Oberman et al. be referenced by an address pointer, as taught by Stroustroup, in order to efficiently and elegantly maintain a value in an array of values.

50. Referring to claim 17, Oberman et al. have taught the method of claim 16, as described above, and further including adjusting at least one of the pointer registers after processing all of the pairs of data elements to account for a number of stages in the pipeline (Figure 50, The output results, elements 3008A and 3008B are adjusted, or set, after elements 204A-D are finished being compared in the required number of pipeline stages necessary to complete the comparison.).

51. Claims 18, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002.

52. While Kobayashi et al. may not have specifically taught issuing N/M machine instructions to a processor, Oberman has taught that the number of instructions are reduced for performing a certain operation when two data elements are compared in parallel. With Oberman we have two separate things that used to be implemented with two instructions, that are now being implemented with one instruction (FPMIN and FPMAX). Implementing half as many instructions of Kobayashi et al. is an obvious improvement in light of Oberman in order to increase instruction parallelism. For example, in the case of Oberman, M=2. If we have an array of Kobayashi of size 10, such that N=10, then 10/2 = 5 instructions would be required to search

the array for an extreme value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al., issue N/M machine instructions to a processor, such that 2 times the amount of data is operated on in a single instruction, as taught by Oberman et al., so that ½ as many instructions of Kobayashi et al. need to be issued to search an array for an extreme value for the desirable purpose of increasing instruction level parallelism and execution time.

53. Referring to claim 24, Oberman et al. have taught the apparatus of claim 18, as described above, and wherein the pipeline includes M accumulators to store M current extreme values (Figure 50, elements 3008A and 3008B).

54. Referring to claim 25, Oberman et al have taught the apparatus of claim 18, as described above, and wherein the pipeline includes M general-purpose registers to store M current extreme values (Figure 50, elements 3008A and 3008B).

Conclusion

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with Every other Friday off.

56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

57. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

tlm
October 30, 2003